

REMARKS

The Examiner is thanked for the indication that claims 13-19 and 28-29 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1-23 and 30-44 are pending in the application. Claims 1, 5, 9, 20, 30, and 41 are independent. By the foregoing Amendment, Applicants have amended claims 1-23, have canceled claims 24-29, and have added claims 30-44. Applicants believe that these changes introduce no new matter and their entry is respectfully requested.

Rejection of Claims 1-12 and 20-27 Under 35 U.S.C. §103(a)

In the Office Action, the Examiner rejected claims 1-12 and 20-27 under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 5,953,685 to Bogin et al. (hereinafter “*Bogin*”) in view of U.S. Patent No. 6,021,076 to Woo et al. (hereinafter “*Woo*”). Applicants respectfully traverse the rejection.

To establish a *prima facie* case of obviousness, an Examiner must show that there is some expectation of success that the combination proffered would result in the claimed invention. The Examiner also must show that the cited references teach each and every element of the claimed invention. (MPEP §2143.) *citing In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). A patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was independently known in the prior art. *KSR Int’l C. v. Teleflex, Inc.*, No 04-1350 (U.S. Apr. 30, 2007). It can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the prior art elements in the manner claimed. (*Id.*)

Embodiments of the present invention operate by increasing bandwidth when accesses to memory are less than anticipated and by decreasing bandwidth when accesses to memory are more than anticipated. According to one embodiment, a computer system has gone into throttle mode and is attempting to reduce power consumption. Normally, to accomplish this, during throttling a memory controller is allocated a certain amount of

accesses and if it exceeds that amount *all* the memory accesses are blocked for a particular period of time. This is how *Bogin* appears to operate. Applicants' Specification also describes this at paragraph [0006].

Embodiments of the present invention allow a memory controller to access memory even after it has reached its allocated bandwidth so that *all accesses are not blocked*. It operates as follows. The less traffic there is during a specific period of time means that less power is consumed. This is rewarded by allowing more traffic in later time periods. Conversely, the more memory traffic during a specific period of time means more power is consumed, which is penalized by allowing less traffic in later time periods. Thus, embodiments of the present invention increase bandwidth when accesses to memory are less than anticipated and decrease bandwidth when accesses to memory are more than anticipated because when accesses to memory are less than anticipated there is more power budget available and so bandwidth can be increased while when accesses to memory are more than anticipated there is less power budget available and bandwidth should be decreased.

Independent claim 1 recites in pertinent part “*increasing the first memory bandwidth if a demand for memory bandwidth is less than the first memory bandwidth*; and decreasing the first memory bandwidth if a demand for memory bandwidth is greater than the first memory bandwidth” (emphasis added). Independent claims 5, 9, and 20 recite similar subject matter.

In the Office Action, the Examiner states that *Bogin* discloses allocating an original percentage of bandwidth or number of access to memory by a memory controller and decreasing the bandwidth or number of access allocated to the memory controller to a percentage lower than an original bandwidth or number of accesses allocated when accesses to memory by the memory controller are more than the original percentage of bandwidth or number of accesses allocated to the memory controller. The Examiner concedes that *Bogin* fails to disclose *increasing* the allocated bandwidth or number of accesses when the actual bandwidth or number of accesses is *less than* the originally allocated bandwidth or number of access but cites *Woo* for disclosing *increasing* the allocated bandwidth or number of

accesses when the actual bandwidth or number of accesses is *less than* the originally allocated bandwidth or number of access. In the Response to Arguments section of the Office Action, the Examiner states that Applicants' arguments are not persuasive because Applicants present arguments that attack the references individually rather as a combination Applicants respectfully disagree.

Neither the *Bogin* patent nor the *Woo* patent, *alone or in combination*, appear to perform the above counterintuitive function. *Bogin* does not disclose variable allocation between first, second, and third bandwidths, but has a fixed allocation pre-programmed at power up of the computer. That is, *Bogin* does not begin with a first bandwidth, increase it to a second bandwidth if memory accesses are lower than anticipated and decreases to a third bandwidth if memory accesses are higher than anticipated. The mask in *Bogin* does not allow the three-way function performed by embodiments of the present invention, but blocks the memory access if the pre-programmed allocation is reached. Thus *Bogin* performs a binary function of only decreasing the bandwidth to a lower value if accesses to memory are more than anticipated, which the Examiner concedes.

Woo also fails to disclose variable allocation between first, second, and third bandwidths. *Woo* appears to teach activating and deactivating a thermal regulation scheme, which is a binary "on" – "off" process, not a three-way process. Assuming for the sake of argument that deactivating the thermal regulation scheme in *Woo* may "increase memory bandwidth," deactivating the thermal regulation scheme in *Woo* **only returns the system in *Woo* back to the original memory bandwidth**. *Woo* does not increase memory bandwidth to a value higher than the original memory bandwidth. Thus, at best, the combination of *Bogin* in view of *Woo* only performs binary allocation. The element of **increasing the memory bandwidth** allocated to the memory controller **to a value higher than the first value if a demand for memory bandwidth by the memory controller is less than the first value** is still missing from the combination of *Bogin* in view of *Woo*.

Thus, Applicants respectfully submit that the combination of *Bogin* and *Woo* fails to teach each and every element of the claimed invention and that the Examiner has failed to

make out a *prima facie* case of obviousness. Claims 24-27 have been canceled rendering the rejection of them moot. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection to claims 1-12 and 20-27.

New Claims 30-44

Applicants respectfully submit that the combination of *Bogin* and *Woo* fails to teach each and every element of new claims 30-44 as well for at least the same reasons that the combination of *Bogin* and *Woo* fails to teach each and every element of claim 1. Accordingly Applicants respectfully submit that claims 30-44 are patentable over *Bogin* and *Woo*.

CONCLUSION

Applicants respectfully submit that all grounds for objection and rejection have been properly traversed, accommodated, or rendered moot, and that the application is now in condition for allowance. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

Respectfully submitted,

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